CLAIMS

What is claimed is:

1. A three-dimensional (3D) integration scheme comprising:

providing a first interconnect structure comprising at least a first semiconductor device located on a surface of a first Si-containing layer of a first silicon-on-insulator substrate, said first Si-containing layer having a first surface orientation that is optimal for said first semiconductor device;

attaching a handling wafer to a surface of the first interconnect structure;

providing a second interconnect structure comprising at least a second semiconductor device that differs from the first semiconductor device on a surface of a second Si-containing layer of a second silicon-on-insulator substrate, said second Si-containing layer having a second surface orientation that is optimal for said second semiconductor device;

bonding the first and second interconnect structures to each other; and

removing the handling wafer.

2. The 3D integration scheme of Claim 1 further comprising forming vertical interconnects between the first and second semiconductor devices.

3. The 3D integration scheme of Claim 2 wherein said step of forming vertical interconnects comprises lithography, etching and deposition of a conductive metal.

4. The 3D integration scheme of Claim 1 wherein said step of attaching comprises applying a polymeric adhesive to a surface of the first interconnect structure, and

bringing the handling wafer and first interconnect structure containing said polymeric adhesive into intimate contact with each other.

5. The 3D integration scheme of Claim 4 further comprising applying an external force to the contacted handling wafer and first interconnect structure containing said polymeric adhesive.

6. The 3D integration scheme of Claim 4 further comprising heating the contacted handling wafer and first interconnect structure containing said polymeric adhesive to a temperature above the melting point of the polymeric adhesive.

7. The 3D integration scheme of Claim 1 wherein the first semiconductor device is a pFET, the first semiconductor layer has a (110) crystallographic orientation, the second semiconductor device is an nFET, and the second semiconductor layer has a (100) crystallographic orientation.

8. The 3D integration scheme of Claim 1 wherein the first semiconductor device is an nFET, the first semiconductor layer has a (100) crystallographic orientation, the second semiconductor device is a pFET, and the second semiconductor layer has a (110) crystallographic orientation.

9. The 3D integration scheme of Claim 1 wherein the step of heating is performed at a temperature from about 200° to about 1050°C for a period of time from about 2 to about 20 hours.

10. The 3D integration scheme of Claim 1 wherein the step of heating is performed in an inert ambient.

11. A 3D integration scheme of the present invention comprising:

bonding a blanket silicon-on-insulator (SOI) substrate having a first SOI layer of a first crystallographic orientation to a surface of a pre-fabricating wafer having at least one second semiconductor device on a second SOI layer that has a different crystallographic orientation than the first SOI layer; and

forming at least one first semiconductor device is said first SOI layer.

12. The 3D integration scheme of Claim 11 further comprising forming vertical interconnects between the first and second semiconductor devices.

13. The 3D integration scheme of Claim 12 wherein said step of forming vertical interconnects comprises lithography, etching and deposition of a conductive metal.

14. The 3D integration scheme of Claim 11 wherein the first semiconductor device is a pFET, the first SOI layer has a (110) crystallographic orientation, the second semiconductor device is an nFET, and the second SOI has a (100) crystallographic orientation.

15. The 3D integration scheme of Claim 11 wherein the first semiconductor device is an nFET, the first SOI has a (100) crystallographic orientation, the second semiconductor device is a pFET, and the second SOI layer has a (110) crystallographic orientation.

16. The 3D integration scheme of Claim 11 wherein the step of bonding is performed at a temperature from about 200° to about 1050°C for a period of time from about 2 to about 20 hours.

17. The 3D integration scheme of Claim 16 wherein the step of bonding is performed in an inert ambient.

18. The 3D integration scheme of Claim 11 wherein the first semiconductor device is formed by a CMOS process.

19. The 3D integration scheme of Claim 11 further comprising a step of removing a bottom Si-containing layer and a buried insulating layer of said blanket SOI substrate after bonding, but prior to said forming step.

20. A three dimensional (3D) integrated circuit comprising:

a first interconnect structure comprising at least a first semiconductor device located on a surface of a first Si-containing layer of a first silicon-on-insulator substrate, said first Si-containing layer having a first surface orientation that is optimal for said first semiconductor device;

a second interconnect structure comprising at least a second semiconductor device that differs from the first semiconductor device located on a surface of a second Si-containing layer of a second silicon-on-insulator substrate, said second Si-containing layer having a second surface orientation that is optimal for said second semiconductor device; and

vertical interconnects connecting the first interconnect structure to the second interconnect structure.

21. The 3D integrated circuit of Claim 20 wherein the first semiconductor device is a pFET, the first semiconductor layer has a (110) crystallographic orientation, the second semiconductor device is an nFET, and the second semiconductor layer has a (100) crystallographic orientation.

22. The 3D integrated circuit of Claim 20 wherein the first semiconductor device is an nFET, the first semiconductor layer has a (100) crystallographic orientation, the second

semiconductor device is a pFET, and the second semiconductor layer has a (110) crystallographic orientation.

23. The 3D integrated circuit of Claim 20 wherein said first and second interconnect structure comprise at least a patterned interconnect dielectric having conductive wiring located therein.